AX99100A PCIe to Multi I/O Application Design Note

Revision 1.00
January 25th, 2024

Revision History

Revision	Date	Description
1.00	2024/01/25	Initial release

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1. Introduction

ASIX Electronics provides the AX99100A single chip solution that fully integrates PCIe 2.0 Gen 1 end-point controller and SerDes with a variety of peripherals such as four High Speed Serial Ports, one Parallel Port, I2C Master, High Speed SPI, Local Bus (ISA-Like) , and GPIOs. It consists of four main configurations such as 4S (PCIe to Quad Serial), 2S+1P (PCIe to Dual Serial and Single Parallel), 2S+SPI (PCIe to Dual Serial and SPI), and LB (PCIe to Local Bus/ISA-Like) for different kinds of applications.

This Application Design Note provides important information about external component selection, schematic design and PCB design/layout for designing with ASIX Electronics PCIe Bridge solutions. ASIX Electronics highly recommends that user read through this Design Note before starting hardware design on schematic capture and PCB layout.

2. Typical Applications Block Diagram

2-1. AX99100A 4S Application Block Diagram

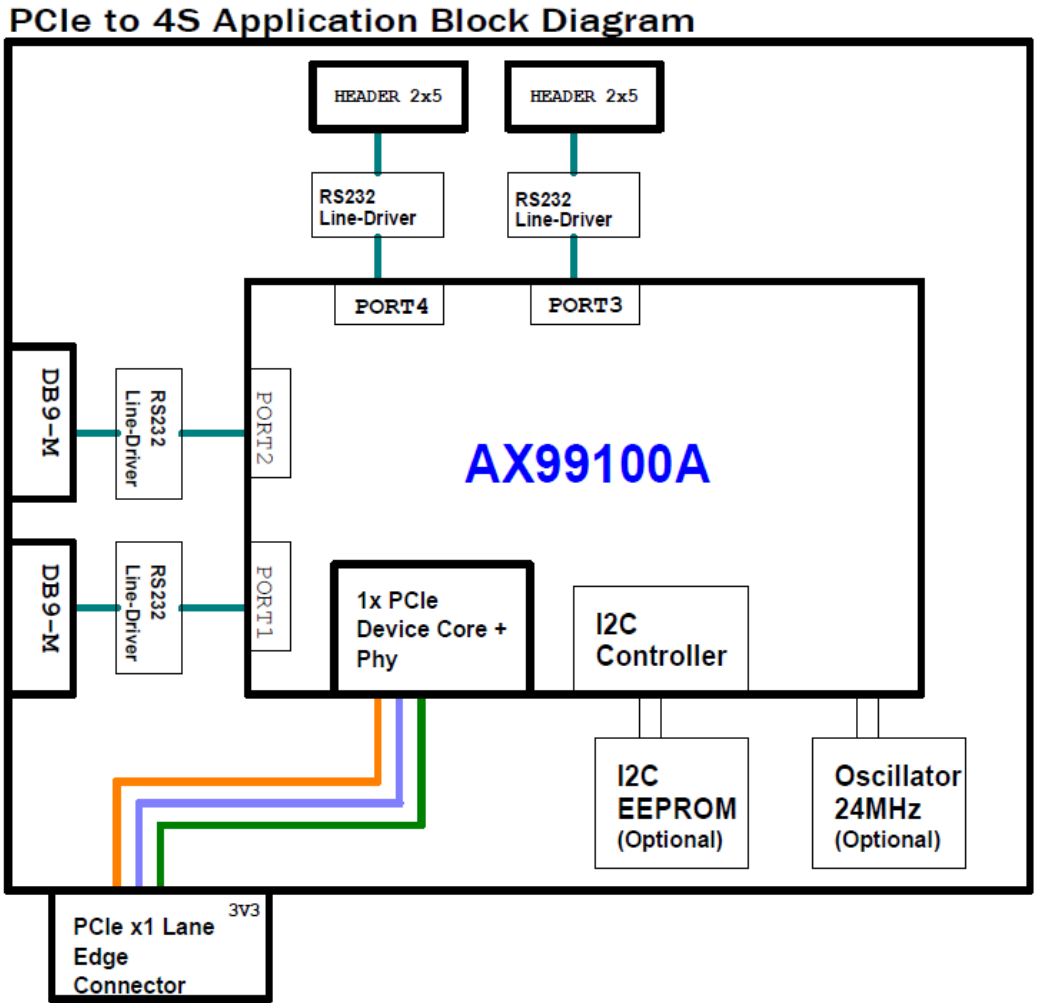


Figure 1. AX99100A 4S Application Block Diagram

2-2. AX99100A 2S1P Application Block Diagram

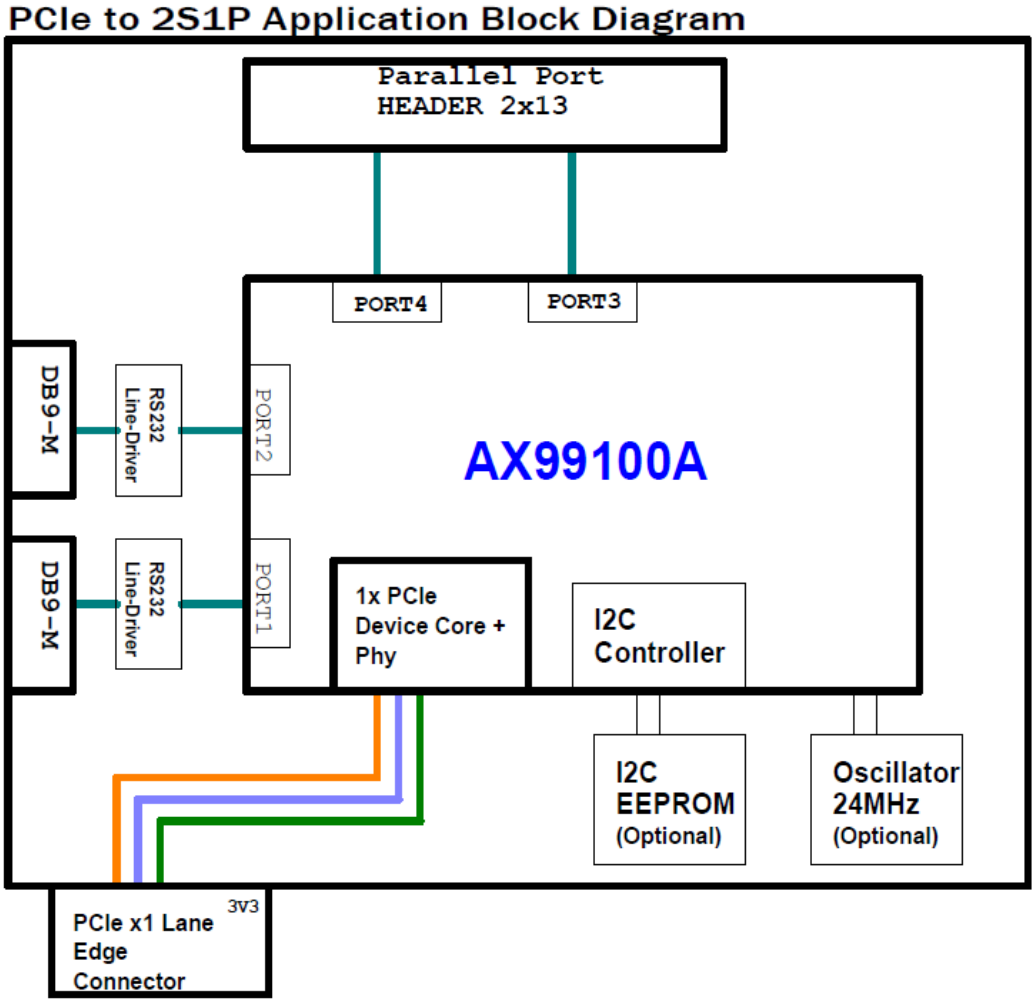


Figure 2. AX99100A 2S1P Application Block Diagram

2-3. AX99100A Local Bus Application Block Diagram

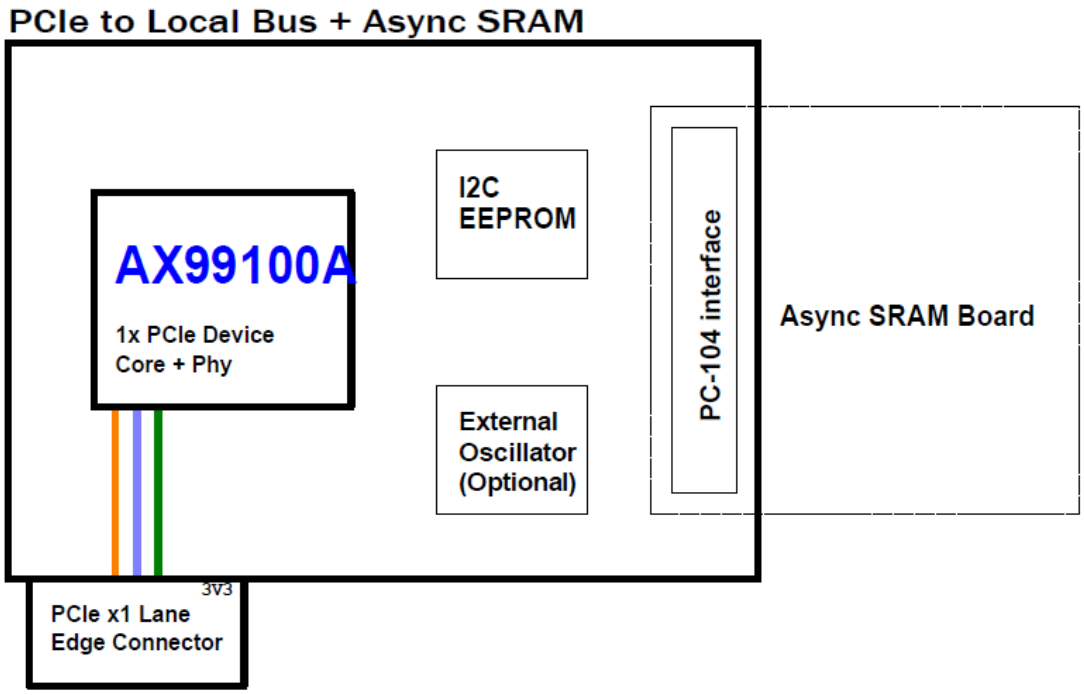


Figure 3. AX99100A Local Bus + Async SRAM Application Block Diagram

2-4. AX99100A 2SSPI Application Block Diagram

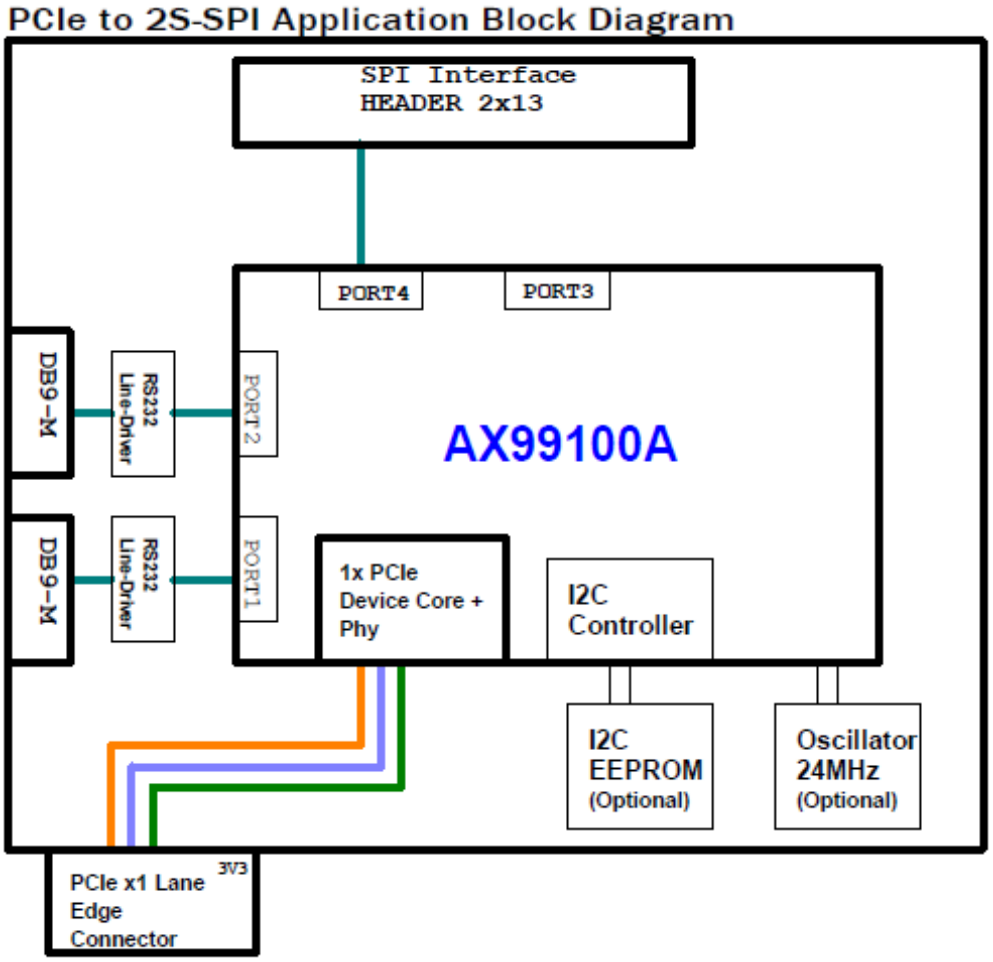


Figure 4. AX99100A 2SSPI Application Block Diagram

3. I2C EEPROM Selection Considerations

The following is the I2C EEPROM reference circuit of AX99100A PCIe to Multi I/O controller and the reference I2C EEPROM parts.

The I2C EEPROM can be optional for some AX99100A standard chip modes applications such as 4S/2S1P/2S1SPI/etc. but is required for some AX99100A applications such as Local Bus/3S/2S/1S/1S1P/etc.

The AX99100A PCIe 2.0 Gen 1 end-point controller supports the 8-bit Addressing mode 24C02 to 24C16 I2C EEPROM with frequency rate up to 400 KHz. The 7-bit device address of the I2C Hardware Configuration EEPROM on AX99100A application circuit MUST be set to **1010000b**.

Please still pull-up SCL and SDA to 3.3v with 4.7k ohm if the EERPOM is empty

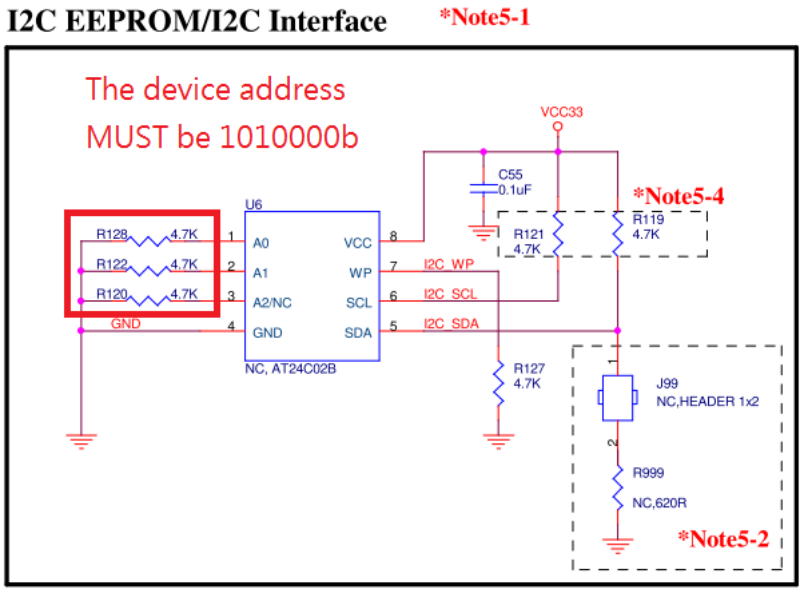


Figure 5. I2C EEPROM Reference Circuit

IMPORTANT!! To program wrong EEPROM contents might cause AX99100A board cannot work normally. Please reserve the I2C_SDA pull-down circuit location on your AX99100A PCB board in order to disable auto-loading I2C EEPROM while AX99100A EEPROM is programmed wrong data.

Vendor	Part Number
ATMEL	AT24C02, AT24C04, AT24C08, AT24C16
STMicroelectronics	M24C02, M24C04, M24C08, M24C16
CATALYST	CAT24C02, CAT24C04, CAT24C08, CAT24C16

Figure 6. Reference I2C EEPROM Parts

4. 4-Layer PCB Design

We strongly suggest customers to design ASIX Electronics' PCIe to Multi I/O on the printed circuit board (PCB) with at least 4 layers. The 4-layer PCB design can help reduce some potential EMI, thermal and signal integrity issues, etc.

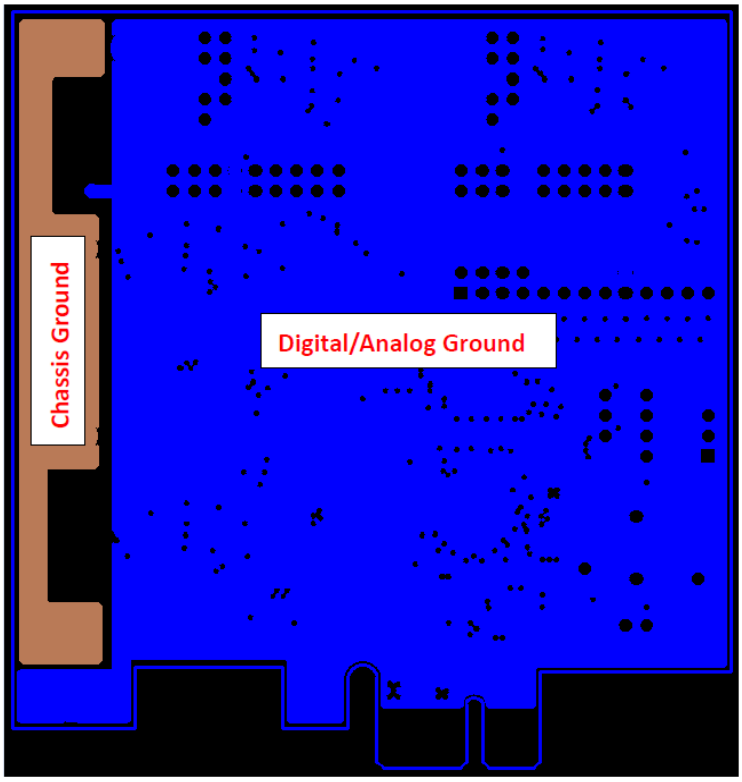
The following is an example 4-Layer PCB design for an embedded system application that uses ASIX Electronics' PCIe to Multi I/O.

Layer 1	Component (Top)	Major Signals
Layer 2	Ground	Ground Planes
Layer 3	Power	Power Planes
Layer 4	Component (Bottom)	Other Signals

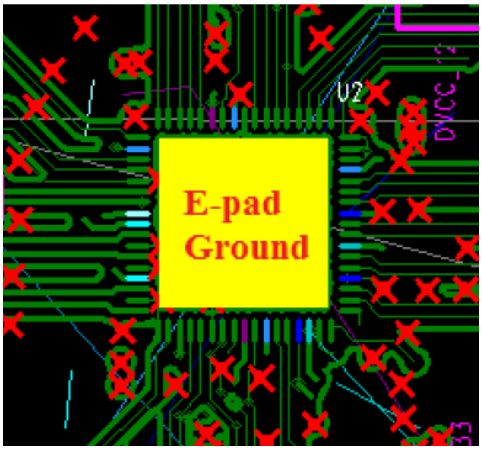
Figure 7. An Example of 4-Lyer PCB Design

5. Power and Ground Planes Considerations

1. Digital GND and Analog GND can be placed together in one-piece so as to enlarge the GND, and thus helping dissipation of noises.



2. Connect AX99100A GNDK E-pad to digital ground plane to reduce AX99100A operating temperature.



3. The RS232 connector chassis ground and the digital ground should be isolated through a Ferrite Bead. And the gap between the chassis ground and digital ground must be wider than 80 mils.

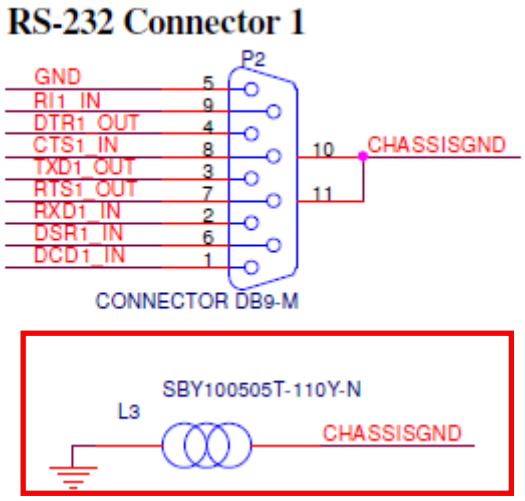
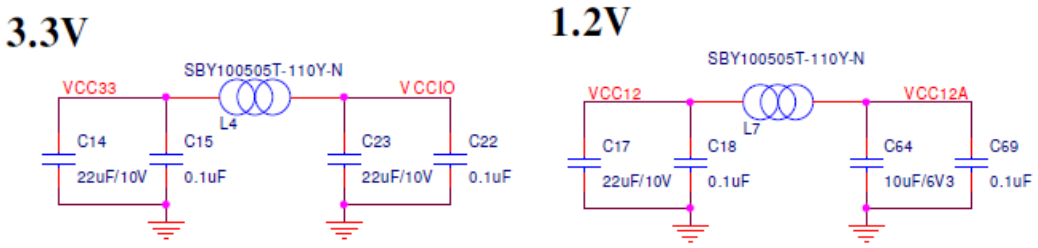


Figure 8. Typical Chassis Reference Circuit

4. The digital and analog power planes should be isolated with a Ferrite Bead to isolate the noise source, and all power planes should be implemented with a large compensating capacitor to provide a stable power source.



5. All the digital and analog power planes for different voltage supplies should be handled separately with different blocks to supply power to IC chip and peripheral components.

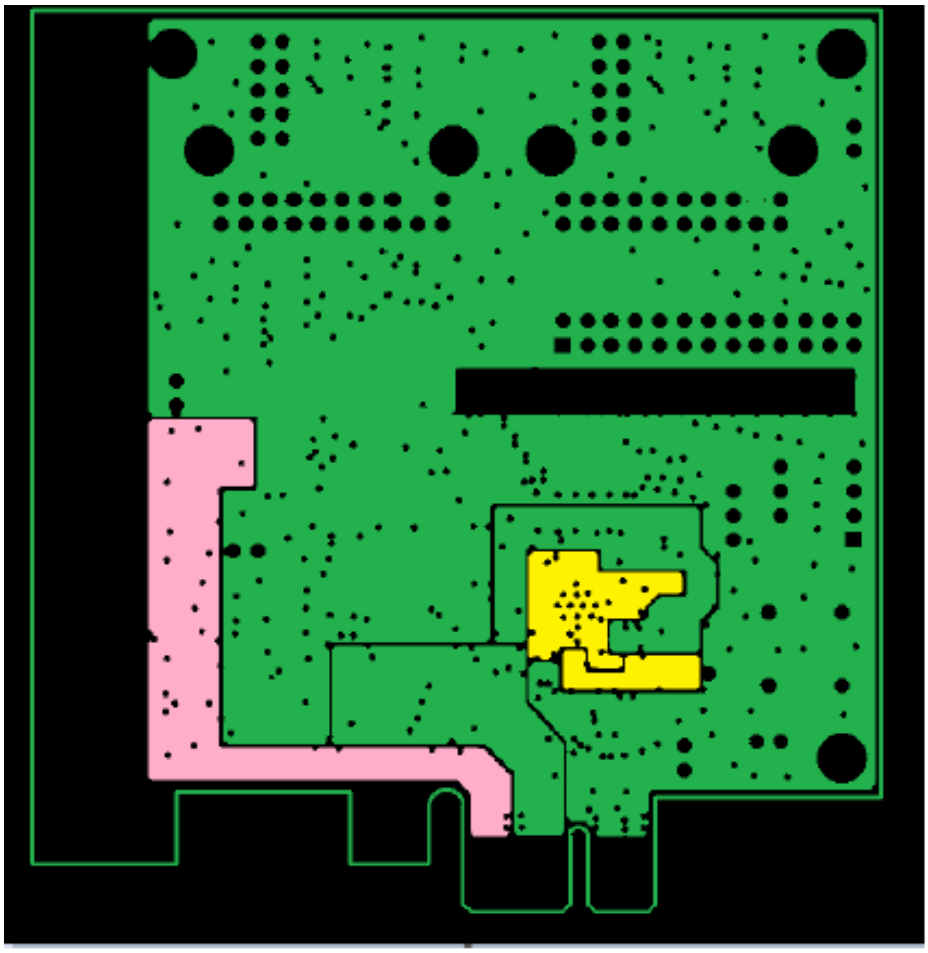


Figure 9. Typical Digital/Analog Power Planes

Note: The above figures are the Digital and Analog Power Planes diagram of an illustrative PCIe board design. For exact layout pattern, ASIX Electronics provides AX99100A demo board PCB layout/Gerber files for customer

6. All power pins should be implemented with a decoupling capacitor, and the decoupling capacitor should be as close to the respective power pin of ASIX PCIe 2.0 Gen 1 end-point controller as possible.

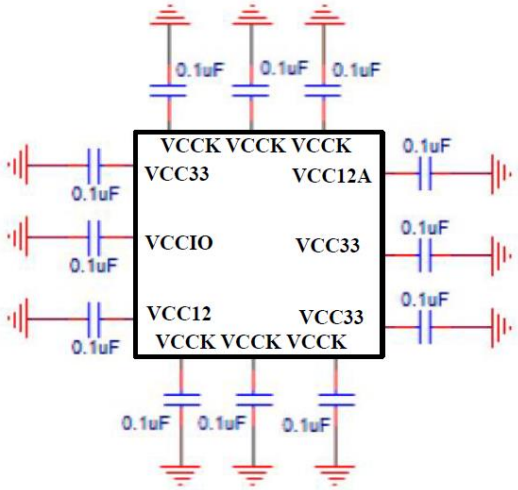
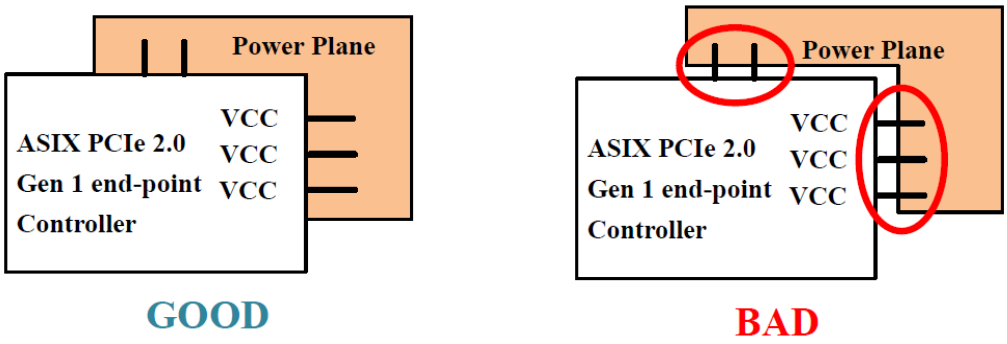


Figure 10. An Example of Power Pins and Decoupling Capacitors Circuits

7. Provide a power plane right underneath the ASIX PCIe 2.0 Gen 1 end-point controller such that the VCC pins can be contacted to the power plane without going through thin traces



6. PCIe Signal Layout Considerations

This section describes some general PCIe signal layout guideline for the differential signals of PCIe interface.

6-1. Differential Pairs

1. TXP and TXN are the differential signals. The layout paths of TXP and TXN need the differential 100-Ω impedances that are matched, balanced, and symmetric. The TXP ball and TXN ball are placed at the outer locations and are parallel to each other.

2. RXP and RXN are the differential signals. The layout paths of RXP and RXN need the differential 100-Ω impedances that are matched, balanced, and symmetric. The RXP ball and RXN ball are placed at the outer locations and are parallel to each other.

3. CLKP and CLKN are the differential signals. The layout paths of CLKP and CLKN need the differential 100-Ω impedances that are matched, balanced, and symmetric. The CLKP ball and CLKN ball are placed at the outer locations and are parallel to each other.

4. The pairs, TXP/TXN, RXP/RXN, and CLKP/CLKN, should be kept away from each other and should be kept away from any toggled digital signal to avoid the noise coupling.

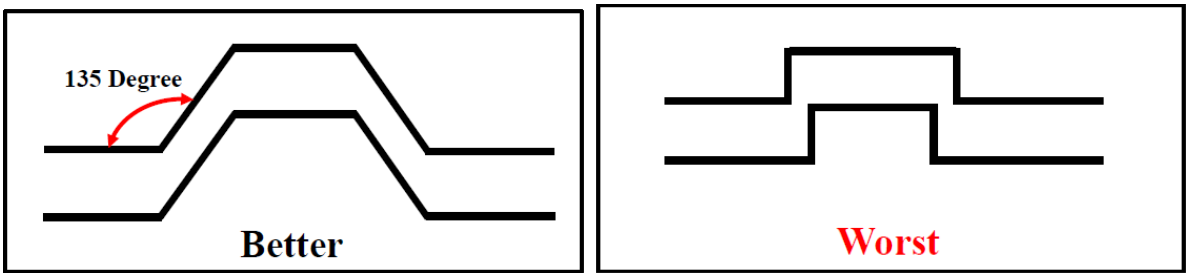
5. The differential signal trace must be length matched to minimize jitter. This length matching requirement applies only to the P and N signals within a differential pair. The transmitter differential pair does not need to be length matched to the receiver differential pair.

6. The differential signal pairs must not be routed over gaps in the power planes or ground planes. This causes impedance mismatches.

7. For the ground plane, please divide it into the analog and digital ground planes. The layout paths of TXP/TXN, RXP/RXN, CLKP/CLKN, and RREF need to be on the analog ground plane.

8. Avoid routing differential pairs adjacent to noisy signals lines or high speed switching devices such as clock chips.

9. The angle of the corner should not be larger than 135 degree in order for the layout path to turn a corner



6-2. Width and Spacing

The coupling of the intra-pair differential signals and increased spacing to neighboring signals help to minimize harmful crosstalk impacts and Electro Magnetic Interference (EMI) effects. The differential trace width and air gap spacing between the two traces of pair need to be elected to achieve the impedance target. Recommended PCI Express microstrip Trace Width/Spacing as below figure.

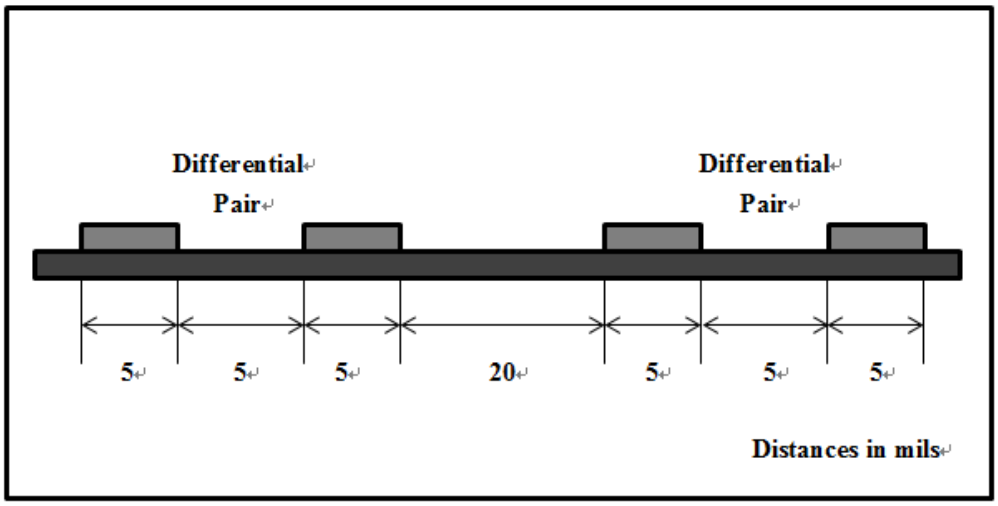


Figure 11. Recommended PCI Express microstrip Trace Width/Spacing.

6-3. Length Matching

The length mismatching between a differential pair should be limited to 5 mils maximum. Length matching is required per segment, and any length added (typically 'serpentine' section) for the sake of matching a pair should be added near the location where the mismatch occurs.

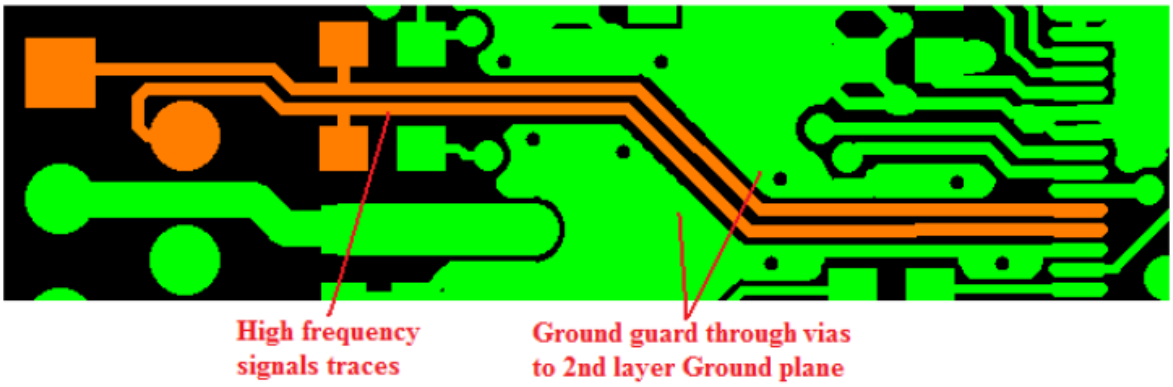
6-4. Routing Rules

The differential signal pairs must not be routed over gaps in the power planes or ground planes. This causes impedance mismatches.

Avoid routing differential pairs adjacent to noisy signals lines or high speed switching devices such as clock chips.

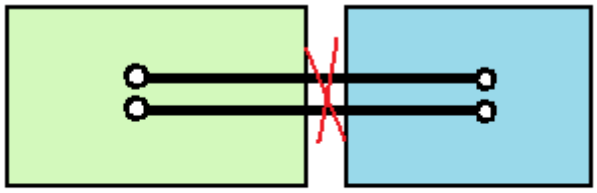
7. EMI Considerations

1. The high frequency signals traces such as PCIe differential signals, clock signals, etc. shall be surrounded by GND to prevent interference to other signal wires. Better EMI effect can be attained by a one-piece GND underneath the IC furnished with PTH holes to enlarge the GND area



2. The chosen connector must be shielded so that EMI integrity of the design is not compromised. The shield must be electrically connected to chassis ground to extend the chassis barrier for high frequency emissions. If an unshielded connector were used, the EMI would pass through the nylon material of the connector. The shield will also prevent less external EMI from entering the chassis.

3. DON'T CROSS ANY SIGNAL TRACES OVER ANY REFERENCE PLANE CUTS. This might cause some unpredictable EMI problems.



4. Essential to maintain the continuous stable ground plane when board design to protect EMI emissions. The PCB designer should look upon the path currents, which take on the ground reference plane, and reduce the loop area. The continuous ground plane helps provide for a low inductance signal return path, and helps maintain a stable power supply. Simply, the most effective method of reducing EMI causes is to decrease the loop area. The main target of ground plane is designed to carry DC current only. Do not use this area as a return path for high speed signals.

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